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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,190	09/30/2003	Myoung-Kee Baek	041993-5348	1266

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EXAMINER

ANYA, IGWE U

ART UNIT PAPER NUMBER

2825

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/673,190

Applicant(s)

BAEK ET AL.

Examiner

Igwe U. Anya

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-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 06092004.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, and 7 – 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuwabara et al. (US Patent 5259926).

3. Kuwabara et al. teach a method of forming a pattern over a substrate, comprising forming a resist layer (3) over substrate (1) having an etching layer (2) thereon, placing a master (4) having a convex surface over the substrate, pressing the master against the substrate to form a same dimension cast on the resist layer and removing the master (figs. 1A – 1D, & col. lines 6 – 47). The etching layer selected from a group comprising of an insulator, silicon oxide, silicon nitride, a semiconductor, and a metal (col. 3 lines 62 – 66). Etching the etching layer using the resist as a mask pattern (fig. 1C, & col. 4 lines 48 – 51) for use in TFT liquid crystal panel (col. 6 lines 61 – 64).

4. Claims 11 – 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Rijn et al. (USPAB 2004/0028875).

5. Van Rijn et al. teach a method of forming a pattern over a substrate (2000), comprising placing a master (2001) having a concave portion over a substrate, forming a resist layer (2003) on the master except for the concave portion, and transferring the resist layer by directly

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contacting the master onto the substrate exposing a portion of the surface over the substrate (Fig. 20A). The resist is a self-aligned monolayer {SAM } (paragraph 184).

6. Claims 16, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Whitesides et al. (5900160).

7. Whitesides et al. teach a method of forming a pattern over a substrate (60), comprising placing a master (20) having a concave portion over a substrate having an etching layer (64), forming a SAM (27) on the master except for the concave portion (col. 14 lines 33 – 35), transferring the SAM by directly contacting the master onto the substrate exposing a portion of the surface over the substrate (Figs. 9), and etching the etching layer using the SAM as a mask pattern (col. 14 lines 21 – 46). The etching layer selected from a group comprising of an insulator, silicon oxide, silicon nitride, a semiconductor, and a metal (col. 15 lines 20 – 38).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

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invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuwabara et al. (US Patent 5259926) in view of Ono et al. (US Patent 5668379).

11. The Kuwabara et al. reference teaches the features previously outlined, but lacks forming a gate electrode and a gate line on the substrate, forming a gate insulating layer on the gate electrode and the gate line, forming a semiconductor layer on the gate insulating layer, forming source/drain electrodes and data line on the semiconductor layer, and forming a passivation layer on the substrate.

12. However, Ono et al. in fig. 3 teach a method a method of forming a TFT-LCD, comprising forming a gate electrode and a gate line (GL) on the substrate, forming a gate insulating layer (GI) on the gate electrode and the gate line, forming a semiconductor layer (AS) on the gate insulating layer, forming source/drain electrodes and data line (DL) on the semiconductor layer, and forming a passivation layer (PSV1) on the substrate (col. 8 line 55 – col. 9 line 30).

13. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Ono et al. into the Kuwabara et al. reference as conventional in the art for forming a TFT-LCD.

14. Claims 4 – 6, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuwabara et al. (US Patent 5259926) in view of Whitesides et al. (5900160).

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15. The Kuwabara et al. reference teaches the features previously outlined, but lacks the resist layer being a SAM layer, forming the SAM comprises dissolving SAM molecules in ethanol, and the SAM having a thickness of tens of angstroms.

16. However, Whitesides et al. teach the resist layer being a SAM layer (fig. 9b element 27), forming the SAM comprises dissolving SAM molecules in ethanol (col. 23 lines 25 – 27).

Regarding the SAM having a thickness of tens of angstroms, where the general conditions are disclosed in prior art, discovering the optimum or working ranges involves only routine skill in the art. (In re Aller, 105 USPQ 233).

17. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Whiteside et al. into the Kuwabara et al. reference to form a patterned substrate with a high degree of accuracy.

18. Prior art considered, but not used in the rejection include Nakashima et al. (US Patent 6162569), Bulchwalter et al. (US Patent 6632536), and Clem et al. (US Patent 6518168).

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Igwe U. Anya whose telephone number is (571) 272-1887. The examiner can normally be reached on M - F 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

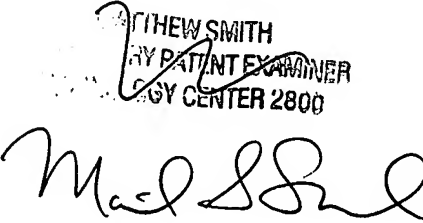
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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Igwe U. Anya  
Examiner  
Art Unit 2825

IA

June 12, 2004

  
MATTHEW SMITH  
ASSISTANT PATENT EXAMINER  
TECHNOLOGY CENTER 2800